REMARKS

This is a full and timely response to the outstanding Final Office Action mailed December 26, 2002 (Paper No. 16). Claims 3-5 are directly amended. Claims 1-10, 17-18, and 20 remain pending in the present application.

Present Status of Patent Application

Claims 1-10, 17-18, and 20 stand rejected under 35 U.S.C. §103(a). Applicants traverse all of the rejections of the Office Action. Reconsideration and allowance of the Application and presently pending claims are respectfully requested.

I. Response to §103 Rejections

Claims 1-5, 17-18 and 20 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Applicant Admitted Prior Art (Figs. 1-2) in view of U.S. Patent No. 6,043,704, to Yoshitake (hereafter *Yoshitake).* Claims 6-10 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Applicant Admitted Prior Art (Figs. 1-2) in view of *Yoshitake* and further in view of U.S. Patent No. 6,140,686, to Mizuno, *et al.* (hereafter *Mizuno*).

In order for a claim to be properly rejected under 35 U.S.C. §103, the combined teachings of the prior art references must suggest all features of the claim invention to one of ordinary skill in the art. See, *e.g., In re Dow Chemical*, 5 USPQ2d 1528, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 USPQ2d 871, 881 (C.C.P.A. 1981). As set forth below, features of the claim invention are not taught or suggested as indicated in the Office Action, and therefore, Applicants respectfully assert that the claims are in condition for allowance.

Claims 1-5, 17-18 and 20

Claim 1 includes "a common area comprising an alignment link for electrically connecting said first port with the said second port; said port extends directly into said common area from a first area; said second port extends directly into said common area from a second area." The Office Action admitted that Applicant Admitted Prior Art (Figs. 1 and 2) fails to disclose the first port extends directly into the common area from a first area. Further, Applicants respectfully submit that the combination of

Applicant Admitted Prior Art and *Yoshitake* fails to teach, disclose or suggest at least the above-quoted elements. In fact, the figures in *Yoshitake* discloses a schematic view of a clock distribution circuitry for a semi-conductor integrated circuit. Applicants respectfully assert that *Yoshitake* fails to teach, disclose or suggest a physical layout and/or placement for aligning ports and providing for a signal buffering within a common area of integrated circuit real estate. In short, *Yoshitake* fails to teach, disclose or suggest a printed circuit board (PCB) layout as disclosed in the Application.

Consequently, the combination of Applicant Admitted Prior Art (Figs. 1 and 2) and *Yoshitake* fails to teach, disclose or suggest "a common area comprising an alignment length for electrically connecting said first port with said second port; said first port extends directly into said common area from a first area; said second port extends directly into said common area from a second area." Applicants respectfully submit that Applicant Admitted Prior Art (Figs. 1 and 2) and *Yoshitake* fails to render claim 1 obvious, and requests that the rejection with withdrawn. Furthermore, Applicants respectfully submit that claims 2-5 are allowable for at least the reason that they depend, either directly or indirectly, from an allowable independent claim. *In re Fine*, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988).

Independent claim 17 includes "a common area comprising an alignment means for electrically connecting said first port with said second port; said first port extends directly into said common area from a first area; and said second port extends directly into said common area from a second area." As mentioned above, with respect to claim 1, Applicants respectfully submit that Applicant Admitted Prior Art (Figs. 1 and 2) and *Yoshitake* fails to render claim 17 obvious, and requests that the rejection with withdrawn. Furthermore, Applicants respectfully submit that claims 18 and 20 are allowable for at least the reason that they depend, either directly or indirectly, from an allowable independent claim. *In re Fine*, supra.

Claims 6-10

Independent claim 6 includes "a common area comprising an alignment link for electrically connecting said first port with said second port; said first port extends directly into said common area from a first area; said second port extends directly into said common area from a second area." The Office Action admitted that Applicant Admitted Prior Art (Figs. 1 and 2) fails to disclose that the first port extends directly

into the common area from a first area. Further, Applicants respectfully submit that the combination of Applicant Admitted Prior Art, *Yoshitake,* and *Mizuno* fails to teach, disclose or suggest at least the above-quoted elements. In fact, as mentioned above with reference to claim 1, *Yoshitake* appears to disclose a schematic view of a clock distribution circuitry for a semi-conductor integrated circuit; whereas, Applicants' Application discloses a physical layout and/or placement on a printed circuit board. In this regard, *Yoshitake* fails to teach, disclose or suggest at least the above-quoted elements.

The Office Action admits that Applicant Admitted Prior Art (Figs. 1 and 2) and *Yoshitake* fail to disclose the integrated circuit real estate comprising multi-levels. While *Mizuno* may disclose more multi-level integrated circuits, *Mizuno* does not remedy the failure of *Yoshitake* and Applicant Admitted Prior Art to disclose all elements of claim 6.

Consequently, Applicant Admitted Prior Art (Figs. 1 and 2), *Yoshitake,* and *Mizuno*, individually or in combination, fail to render claim 6 obvious. In this regard, Applicants respectfully request allowance of claim 6 and that the rejection withdrawn. Furthermore, Applicants respectfully submit that claims 7-10 are allowable for at least the reason that they depend, either directly or indirectly, from an allowable independent claim. *In re Fine,* supra.

Response to Claim Objections Regarding Claims 3-5

Claims 3-5 have been amended to include Examiner's suggested changes. Therefore, Applicants respectfully submit that claims 3-5 are now in condition for allowance and that the objection be withdrawn.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-10, 17-18 and 20 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite

the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, Washington D.C. 20231, on Feb. 5, 2003.

Anne Antonoff

ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

The following is a marked up version of the amended claims. Amend the following claims by adding the language that is underlined ("___") and by deleting the language that is enclosed within brackets ("[ ]"):

3. (Once Amended) An integrated circuit according to claim 1 wherein said alignment link comprises [a] said common area of integrated circuit real estate.

4. (Once Amended) An integrated circuit according to claim 1 wherein said first port is located in [a] said first area of integrated circuit real estate.

5. (Once Amended) An integrated circuit according to claim 1 wherein said second port is located in [a] said second area of integrated circuit real estate.